ABSTRACT OF THE DISCLOSURE

A method of manufacturing a semiconductor memory integrated circuit intended to improve properties and reliability of its peripheral circuit includes the step of forming a tunnel oxide film (21a) in the cell array region, gate oxide film (21b) for a high-voltage circuit and gate oxide film (21c) for a low-voltage circuit both in the peripheral circuit to respectively optimum values of thickness, and covering them with a first-layer polycrystalline silicon film (22). After that, device isolation grooves (13) are formed and buried with a device isolation insulating film (14). The first-layer polycrystalline silicon film (24) is a non-doped film, and after device isolation, a second-layer polycrystalline silicon film (24) is doped with phosphorus in the cell array region to form floating gates made of the first-layer polycrystalline silicon film (22) and the second-layer polycrystalline silicon film (24). In the peripheral circuit, gate electrodes are made of a multi-layered film including the first-layer polycrystalline silicon film (22), second-layer polycrystalline silicon film (24) and third-layer polycrystalline silicon film 28, and impurities are ion implanted thereafter to respective transistor regions under respectively optimum conditions.